



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

MW

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,904	09/18/2003	Randy L. Schnepper	501323.01	7038
7590	08/23/2006			EXAMINER PORTKA, GARY J
Kimton N. Eng, Esq. DORSEY & WHITNEY LLP Suite 3400 1420 Fifth Avenue Seattle, WA 98101			ART UNIT 2188	PAPER NUMBER
			DATE MAILED: 08/23/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/665,904	SCHNEPPER, RANDY L.
	Examiner	Art Unit
	Gary J. Portka	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 July 2006.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 5,12,18,24,35,36,38,39,41-44,46-48 and 50-60 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 5,24,35,36,47,48 and 50 is/are allowed.
- 6) Claim(s) 12,18,38,39,41-44,46 and 51-60 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>various</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. Claims 1-4, 6-11, 13-17, 19-23, 25-34, 37, 40, 45, and 49 were canceled, and claims 5, 12, 18, 24, 35, 38, 41, 43, 44, 47, 51, and 57 were amended by Applicant. Claims 5, 12, 18, 24, 35, 36, 38, 39, 41-44, 46-48, and 50-60 are pending.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on various dates were considered by the examiner, although the excessive number of documents contained therein prevented the examiner from doing anything more than a cursory inspection thereof.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 38-39, 41-44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf, in view of the admitted prior art.

5. As to claims 38, 41-43, and 46, Langendorf discloses a memory hub, subsystem, and module (see Abstract, Fig. 2) comprising high-speed interface for receiving memory access requests (at 205, 208, and 210), non-volatile memory having memory configuration information (BIOS), memory controller coupled to the above having registers into which the information is loaded, and operable in accordance therewith (at 300, Fig. 3, also see col. 2 lines 35-41, col. 5 lines 18-29 and 36-43). Langendorf does

not disclose the serial bus as recited. However, Applicant has admitted that such a bus was prior art (see pages 6-7 of the specification). An artisan would have been motivated to use a serial bus because of well known art advantages of reducing size and cost, as well as to utilize existing configurations using this bus. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a serial bus, because they were well known to reduce size and cost, and were admitted as prior art.

6. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf in view of the admitted prior art, and further in view of Dodd et al., US 6,952,745 B1 (hereinafter "Dodd").

7. As to claims 12 and 18, Langendorf does not disclose the memory is SDRAM. However, such memory was well known, and was disclosed in a similar memory/controller device as taught by Dodd, see col. 2 line 34 to col. 3 line 25. It would have been obvious to one of ordinary skill in the art at the time of the invention to use SDRAM, because it was a widely known and used memory that can achieve improved performance, and was known in similar memory/controller systems.

8. Claims 51-52 and 54-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf. Alternatively, claims 51-52 and 54-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf in view of Jeddeloh.

9. As to claims 51-52 and 54-58, Langendorf discloses a memory hub, sub-system, and module (see Abstract, Fig. 2) comprising high-speed interface for receiving memory access requests (at 205, 208, and 210), non-volatile memory having memory

configuration information (BIOS), memory controller coupled to the above having registers into which the information is loaded, and operable in accordance therewith (at 300, Fig. 3, also see col. 2 lines 35-41, col. 5 lines 18-29 and 36-43). Langendorf does not disclose a plurality of non-volatile memories each copying to a respective memory controller. However, it would have been clearly obvious to an artisan to use the teachings of Langendorf in any number of instances; that is, the teaching is scalable. For example, the teaching is applicable to each node of a system that has multiple nodes, where one node is equivalent to the Langendorf Fig. 1. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have plural non-volatile memories and respective plural memory controllers, because the teachings in Langendorf are applicable to any number of like systems.

10. Alternatively, Jeddeloh discloses a system having multiple processor and multiple memory controllers (Fig. 4) each having registers loaded from non-volatile memory. Each location from which configuration data is retrieved may be considered a non-volatile memory to the extent recited. That is, configuration data must come from a program or control data that was stored in a nonvolatile manner on ROM or disk, since it would have been lost if otherwise. Also, it is desirable to have multiple BIOS load multiple controllers since there are multiple processors and this would certainly initialize the controllers faster. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use multiple non-volatile memories to load multiple controllers, because this was taught by Jeddeloh, and would be the fastest way to initialize them.

Art Unit: 2188

11. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf, in view of the admitted prior art, or alternatively over Langendorf and Jeddelloh, in view of the admitted prior art.

12. As to claim 53, Langendorf does not disclose the serial bus as recited. However, Applicant has admitted that such a bus was prior art (see pages 6-7 of the specification). An artisan would have been motivated to use a serial bus because of well known art advantages of reducing size and cost, as well as to utilize existing configurations using this bus. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a serial bus, because they were well known to reduce size and cost, and were admitted as prior art.

13. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf in view of Dodd, or alternatively over Langendorf and Jeddelloh, in view of Dodd.

14. As to claim 59, Langendorf does not disclose that the configuration loads capacity or clock speed. However, in a similar memory controller loading system, Dodd teaches to load a memory controller with memory characteristics stored in a non-volatile memory, including memory size (capacity) as well as other characteristics. It would have been obvious to one of ordinary skill in the art at the time of the invention to load capacity or clock speed, because it was known to be useful in similar memory/controller systems.

15. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Langendorf, or over Langendorf in view of Jeddelloh.

Art Unit: 2188

16. As to claims 39, 44, and 60, Langendorf does not disclose the non-volatile memory integrated with the controller. However, integration or relocation of elements absent any functional result is not generally afforded patentable weight, since such integration/relocation is obvious. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the non-volatile memory and the controller, because was known to reduce size, complexity, and likely reduce cost and improve performance.

Allowable Subject Matter

17. Claims 5, 24, 35, 36, 47, 48, and 50 are allowed.

Response to Arguments

18. Applicant's arguments filed July 3, 2006 have been fully considered but they are not persuasive. Applicants have argued that the BIOS of Langendorf is not included in the memory hub. However, there is no structural limitation of the claim that prevents it from being interpreted as such. The BIOS meets the functional limitations of the claim, and thus may be considered a part of the hub to the extent claimed. Applicant argues that Langendorf does not disclose a configuration memory coupled to a host via a local serial bus and to a memory controller through a configuration path. However, the configuration memory (BIOS) of Langendorf is coupled to the memory controller via a configuration path, and the serial bus as noted in the rejection above is admitted as prior art. Applicant argues that there is no motivation to scale Langendorf as stated in the rejection, that such scaling would result in multiple memory domains with respective controllers, and that there would be no reason to include multiple ROMs. However, as

Art Unit: 2188

previously stated, the teachings of Langendorf clearly apply to any number of systems such as multiple independent computers, which individually are advantageously combined via any number of networking or buss arrangements. For example, several systems like that shown in Langendorf may be advantageously connected via a network for communication, data sharing, or other well known purposes, this combination well known in the art and reading on the present claims 51 and 57.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

Art Unit: 2188

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

August 21, 2006



GARY PORTKA
PRIMARY EXAMINER